



Who are we

Flow

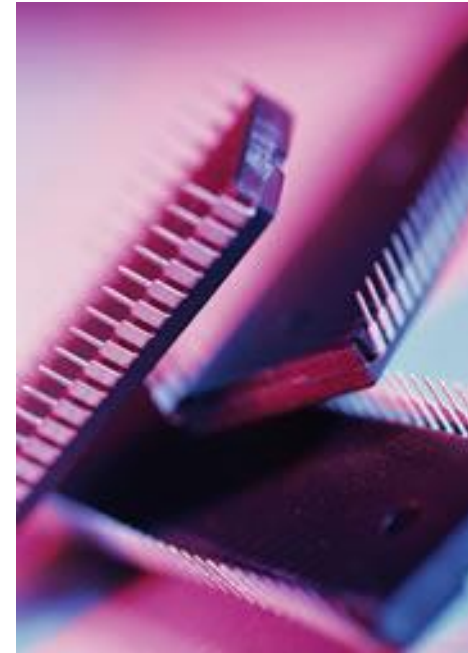
Example

Timeline

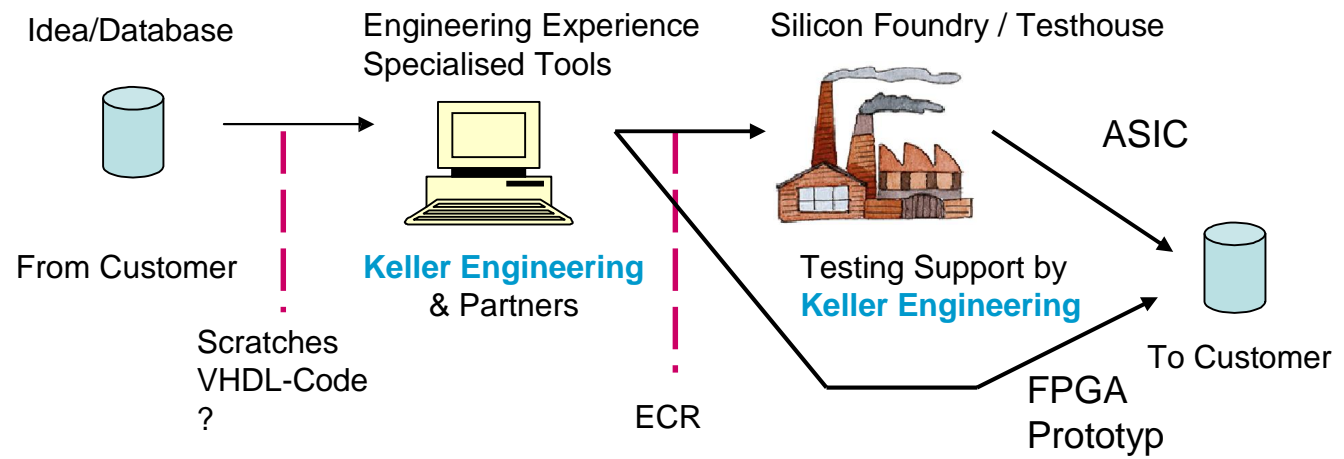
## ***Keller Engineering is «fab-less» Designhouse***

*Expert in FPGA/ASIC Design  
and Verification:*

- *From Idea to Working Silicon*
- *small and middle Volumes*
- *Mixed Signal and digital*
- *Afterlifemanagement*
- *Testing*



## ***From Idea to Working Silicon***



- *20 Years Experience in Microelectronics*
- *Most actual Development Software*
- *Technology independent Development*
- *Excellent Relations to Silicon Fabs and Testhouses*



Who are we

Flow

Example

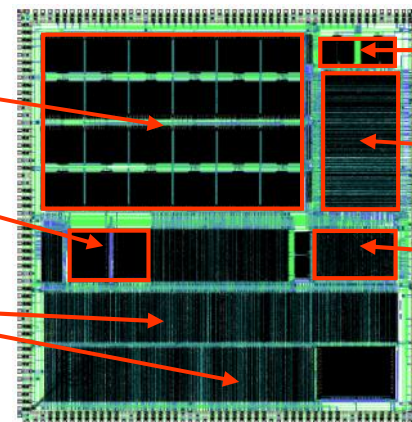
Timeline

## ***Example***

**SRAM**  
4 \* 6 \* 1k x 8

**FIFO**  
2 \* 0.5k x 16

**Random  
Logic**



**ROM**  
2 \* 2k x 32

**ARM  
V6 Core**

**DPSRAM**  
1k x 16

← 8.4 mm →

- ***ARM V6 Core***
- ***150'000 Gates***
- ***RAM : 28 kB***
- ***ROM : 16 kB***
- ***Process : XFAB CX06 3LM***



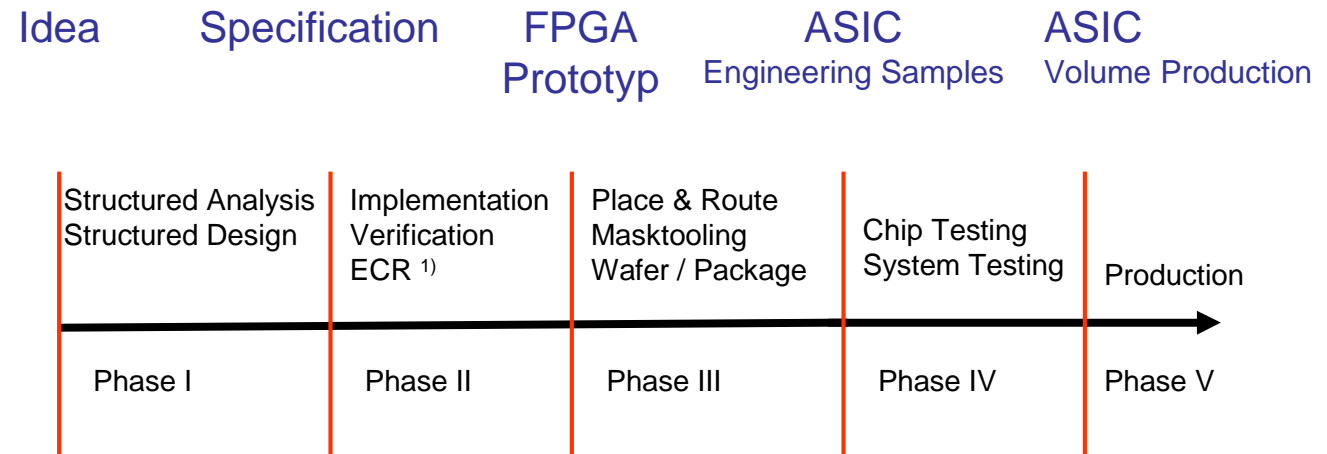
Who are we

Flow

Example

Timeline

## ***Timeline***



<sup>1)</sup> Engineering Completion Report